DIGITAL LOGIC DESIGN / DIGITAL ELECTRONIC

Course Code: ENT262/ENT263

Number of Unit: 4

Course Type: CORE

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COURSE SYNOPSIS

- This course provides the fundamental theory of digital logic design.
- It introduces the basic principle of digital electronics which covers the numbering systems, codes, logic gates, Boolean Algebra and logic simplification.
- The course also introduces to logic design, particularly in combinational logic functions, bi-stable memory devices, sequential circuits design, programmable logic and memory units

LIST OF EXPERIMENTS

1. Logic Gates
2. Combinational Logic Circuits
3. Seven Segment Decoder
4. Multiplexer and Demultiplexer
5. Flip-flops and Latches
6. Counter

LEARNING APPROACH

- Lecture – 45 hours
- Laboratory – 12 hours
- Tutorial – 6 hours
- Mini Project – 6 hour

COURSE OUTCOME MATRIX

Course Outcome (CO)	Domain and Taxonomy Levels	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	Possible Assessment
CO1: Ability to describe, apply and analyze digital electronic components.	**C4**	✓	✓											Quizzes, Assignments, Examination
CO2: Ability to analyze and evaluate digital logic circuits.	**C5**	✓	✓											Quizzes, Assignments, Examination
CO3: Ability to design digital logic circuits to meet any given specifications.	**C6 P4 A3**	✓	✓	✓	✓	✓				✓	✓			Quizzes, Assignments, Examination, Mini Project

TIMETABLE

	PPKM - NORASMADI BIN ABDUL RAHIM																	
	08:00-08:30	08:30-09:00	09:00-09:30	09:30-10:00	10:00-10:30	10:30-11:00	11:00-11:30	11:30-12:00	12:00-12:30	12:30-13:00	13:00-13:30	13:30-14:00	14:00-14:30	14:30-15:00	15:00-15:30	15:30-16:00	16:00-16:30	16:30-17:00
Monday	---	---	---	---	---	--- L	---	---	---	---	---	---	---	---	---	---	---	---
Tuesday	PPKM - MUHAMMAD JUHAIRI AZIZ BIN SAFAR, PPKM - NORASMADI BIN ABDUL RAHIM RK24 - Y2G2, RK24 - Y2ExDipG2 ENT262 - Digital Logic Design LAB RK24 - MN4B1 PPKM - Lab MN4B1				PPKM - NORASMADI BIN ABDUL RAHIM, PPKM - MUHAMMAD JUHAIRI AZIZ BIN SAFAR RK24 - Y2G1, RK24 - Y2G2, RK24 - Y2ExDipG1, RK24 - Y2ExDipG2 ENT262 - Digital Logic Design Lecture (B) - RK24 PPKM - BKN 6&7				---	---	PPKM - MUHAMMAD JUHAIRI AZIZ BIN SAFAR, PPKM - NORASMADI BIN ABDUL RAHIM RK24 - Y2ExDipG1, RK24 - Y2G1 ENT262 - Digital Logic Design LAB RK24 - MN4B1 PPKM - Lab MN4B1				---	---	---	---
Wednesday	---	---	---	---	---	---	---	---	---	---	---	---	---	--- L	PPKM - NORASMADI BIN ABDUL RAHIM, PPKM - MUHAMMAD JUHAIRI AZIZ BIN SAFAR RK24 - Y2G1, RK24 - Y2G2, RK24 - Y2ExDipG1, RK24 - Y2ExDipG2 ENT262 - Digital Logic Design Lecture (B) - RK24 PPKM - DKN 1&2			
Thursday	---	PPKM - MUHAMMAD JUHAIRI AZIZ BIN SAFAR, PPKM - NORASMADI BIN ABDUL RAHIM RK24 - Y2G1, RK24 - Y2G2 ENT262 - Digital Logic Design LAB RK24 - MN4B1 PPKM - Lab MN4B1				---	---	---	---	---	---	---	---	---	---	---	---	---
Friday	---	---	---	---	---	---	---	---	-X-	-X-	-X-	-X-	-X-	-X-	---	---	---	---
	Timetable generated with FET 5.38.1 on 8/30/19 5:10 PM																	

TEACHING PLAN GUIDE

Semester 1, 2019/2020

Minggu/ Study Week	**Kandungan Kursus/** Course Content	**Mod Penyampaian /** Delivery Mode	**Tahap Kesukaran/** Level of Complexity	**Penilaian Dicadangkan/** *Possible Assessments*
1-2	**<u>Introduction to Digital System and Number Systems</u>** **Explain** the basic differences between digital and analoq quantities. **Describe** the representation of voltage levels as digital quantities and various parameters of a pulse waveform. **Express** and **convert** the numbers using decimal, binary, octal, hexadecimal, BCD and gray codes. **Determine** the 1's and 2's complement of binary numbers. **Express** signed binary numbers and **apply** arithmetic operations. **(7 Hours)**	Lecture	C3: Application	Quizzes Assignments Examination
	Tutorial 1 **(2 Hours)**	Problem Solving		
3	**<u>Logic Gates</u>** **Describe** the operation of logic gates and **express** it with Boolean Algebra and truth-table. **Use** the logic gates in simple digital electronic applications. **Construct** simple combinational logic circuits. **(3 Hours)**	Lecture	C3: Application	Quizzes Assignments Examination
	Laboratory 1 **(2 Hours)**	Laboratory	C3: Application	Reports

4-5	**Boolean Algebra and Logic Simplification** **Apply** the basic laws and rules of Boolean algebra and DeMorgan's theorems. **Analyze** and **simplify** the Boolean expressions. **Express** the Boolean expression into sum-of-products (SOP) and products-of-sum (POS) form. **Relate** the Boolean expression to truth-table. **Apply** the Karnaugh map for simplifying Boolean expressions. **(6 Hours)**	Lecture	C4: Analysis	Quizzes Assignments Examination
	Laboratory 2 **(2 Hours)**	Laboratory	C3: Application	Reports
	Laboratory 3 **(2 Hours)**	Laboratory	C3: Application	Reports
6-7	**Combinational Logic Circuits** **Describe** and **analyze** combinational logic circuits. **Express** combinational logic circuits with Boolean expression. **Design** logic circuits based on Boolean expressions and **simplify** the logic circuits. **Design** logic circuits based on SOP and POS forms. **Design** and **evaluate** logic circuits based on given specifications. **(6 Hours)**	Lecture	C6: Evaluation	Quizzes Assignments Examination
	Tutorial 2 **(2 Hours)**	Problem Solving		
	Laboratory 4 **(2 Hours)**	Laboratory	C3: Application	Reports
8	**CUTI PERTENGAHAN SEMESTER** / *MID SEMESTER BREAK*			

9	**<u>Functions of Combinational Logic Circuits</u>** **Explain** the concepts of half-adder, full-adder and comparators. **Design** and **implement** binary and BCD-to-7-segment decoders. **Explain** and **apply** multiplexers and demultiplexers. **(3 Hours)**	Lecture	C5: Synthesis	Quizzes Assignments Examination
	Laboratory 5 **(2 Hours)**	Laboratory	C3: Application	Reports
10-11	**<u>Bistable Memory Devices</u>** **Construct** latches and flip-flops using basic logic gates. **Recognize** the differences between the latches and flip-flops. **Apply** and **analyze** flip-flops in basic applications. **(8 Hours)**	Lecture	C4: Analysis	Quizzes Assignments Examination
12-13	**<u>Sequential Circuits</u>** **Explain** the concepts of shift registers, asynchronous counters and synchronous counters. **Design** and **evaluate** the sequential circuits based on given specifications. **(6 Hours)**	Lecture	C6: Evaluation	Quizzes Assignments Examination
	Tutorial 3 **(2 Hours)**	Problem Solving		
	Laboratory 6 **(2 Hours)**	Laboratory	C3: Application	Reports

14	**Programmable Logic** **Discuss t**he types of programmable logic, Simple Programmable Logic Devices (SPLDs), Complex Programmable Logic Devices (CPLDs) and Field-Programmable Gate Arrays (FPGA), and **explain** their basic structures. Distinguish between CPLDs and FPGAs. **Explain** the design flow of programmable logic. **(3 Hours)**	Lecture	C2: Comprehension	Quizzes Assignments Examination
	Mini Project **(3 Hours)**	Mini Project	C6: Evaluation P4: Mechanism A3: Valuing	Reports Presentation
15	**Data Storage** **Define** the basic memory characteristics. Explain the Random-Access Memory (RAM), Read-Only Memory (ROM) and **differentiate** their functions. Describe the flash memory, magnetic and optical storage technology. **(3 Hours)**	Lecture	C2: Comprehension	Quizzes Assignments Examination
	Mini Project **(3 Hours)**	Mini Project	C6: Evaluation P4: Mechanism A3: Valuing	Reports Presentation
16	**MINGGU ULANGKAJI** / *REVISION WEEK*			
17-19	**PEPERIKSAAN AKHIR SEMESTER** / *FINAL EXAMINATION*			

(12) **Sumbangan Penilaian**/ *Evaluation contribution:*

(i) **Peperiksaan**/ *Examination:* 70%

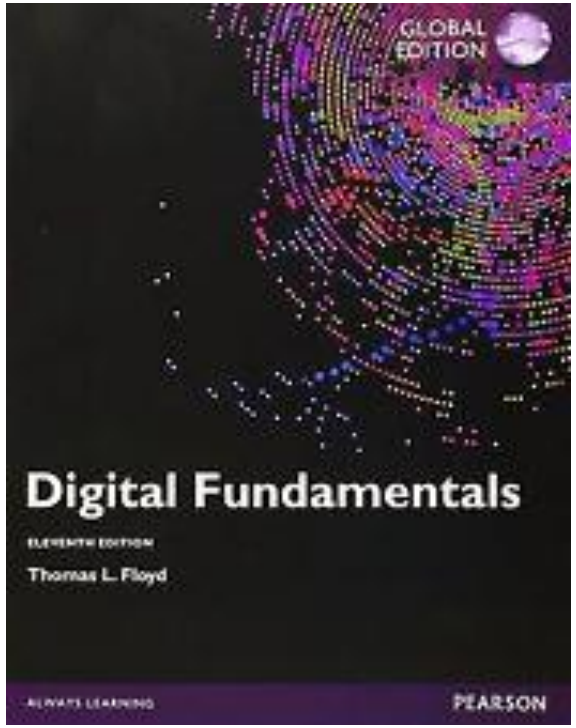
- Peperiksaan Pertengahan Semester/*Mid Term Examinations* = 10%
- Peperiksaan Akhir/ *Final Examination* = 60%

(ii) **Penilaian Berterusan**/ Continual Assessment: 30%

- Kuiz /*Quizzes*
- Tugasan/*Assignment*
- Laboratory/ *Amali*
- Mini Project/ *Projek Mini*

REFERENCE BOOK

- Thomas L. Floyd, "Digital Fundamentals", 11th Ed., Pearson, 2015.
- M. Morris R. Mano, Charles R. Kime, Tom Martin, "Logic & Computer Design Fundamentals", 5th Ed., Pearson, 2016.
- Alan Marcovitz, "Introduction to Logic Design", 3rd Ed., McGraw Hill, 2010.



WARNING AND BARRING

Student attendance must be >80%

Student absentees >20%, without valid reason could be barred

UNIVERSITI MALAYSIA PERLIS

CONDITION FOR PASSING THE COURSE

EAC Requirement:

*"The IHLs must ensure that **no students shall pass a course** if they **fail in their final examination** of that course, unless the **continuous assessment** approach adopted **can demonstrate the attainment of the depth of knowledge.**"*

FE : Final Exam

MTE : Mid Term Exam

CW : Course Work

Prepared by:
Academic Management Division, Universiti Malaysia Perlis (UniMAP)

Applicable to :

All Bachelor of Engineering Students

Courses involved:

All B. Eng core courses that have FE

Conditions:

If FE marks < 40%

Overall Marks = FE Marks

If FE marks ≥ 40%

Overall Marks = FE + MTE + CW

FE Passing Marks:

40%

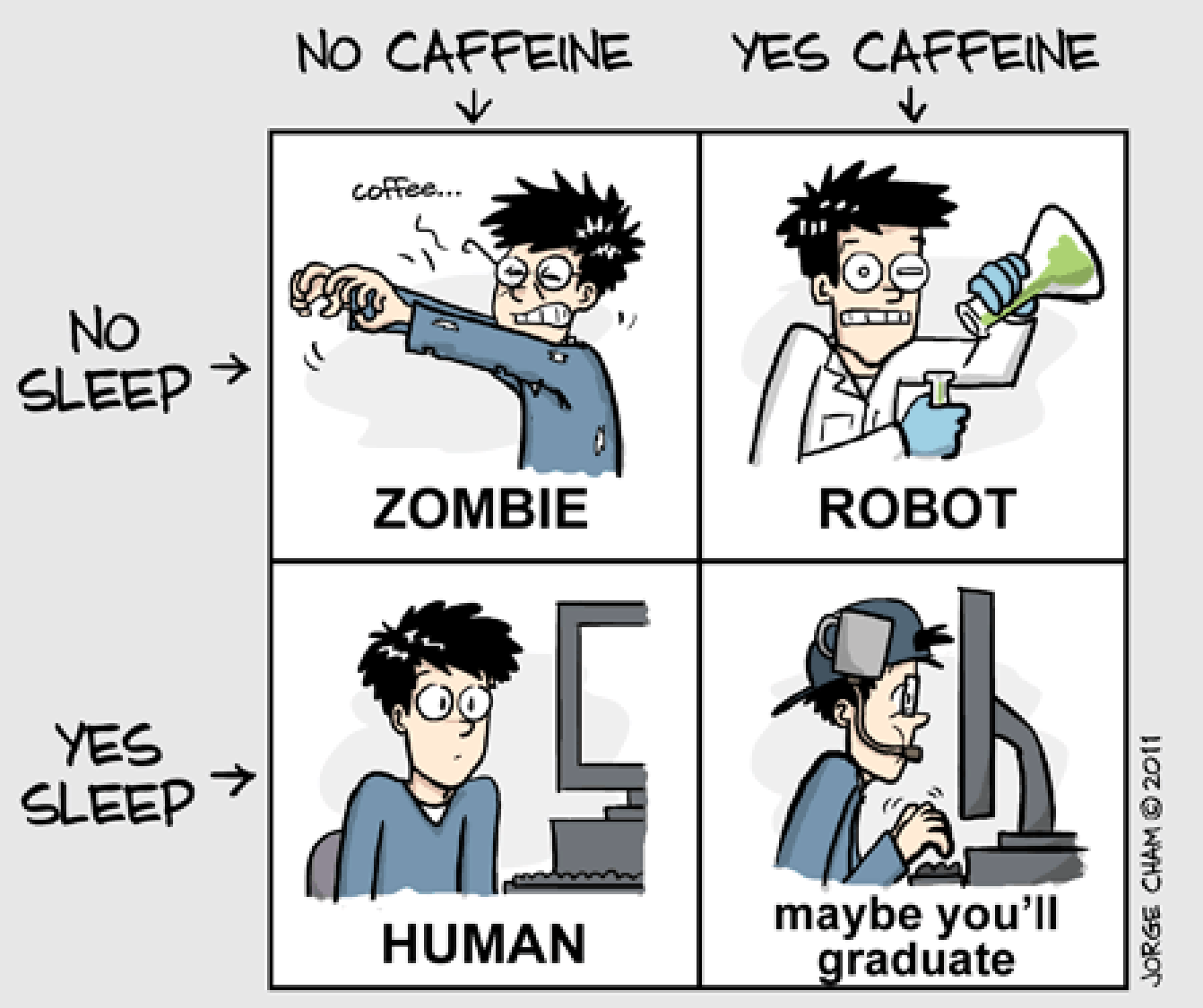
Effective from:

Sem 1 2019/2020

Examples:

Components	%
FE	50
MTE	20
CW	30

Component	Case 1	Case 2
FE	35/100	40/100
MTE	20/20	20/20
CW	30/30	30/30
Overall Marks	35/100	$\frac{40}{100}(50)+20+30=\frac{70}{100}$
Overall Grade	D	B+



ENERGY LEVELS

Reference: http://www.phdcomics.com/comics/archive.php?comicid=1415