MARKS	
DEMO:	
PART A:	/10
PART B:	/10
PART C:	/10
REPORT:	/20

ENT 262
DIGITAL LOGIC DESIGN
SEMESTER 1 2019/2020

LABORATORY 3

HALF AND FULL-ADDERS

Student's Particular

Name:
Matrix No.:
Group:
Date of Experiment:
Breadboard No.:

LAB 3: Half and Full-Adders

OBJECTIVES

1. To construct a half-adder from the basic gates
2. To construct a full-adder from two half-adders
3. To construct 2-bit parallel full-adder.

EQUIPMENTS/COMPONENTS

- A DC power supply capable of 5V DC output
- A multimeter
- Logic gates (74xx-series)
- Light Emitting Diodes (LED) (3 Units)
- 330 Ω resistor (3 Units)
- Switches (4 Units)

INTRODUCTION

Binary arithmetic is essential in all digital computers and in many other types of digital systems. To understand digital systems, you must know the basics of binary addition, subtraction, multiplication and division. An interesting arithmetic is in binary addition. Binary addition has four basic rules for adding a binary digit as follows:

0 + 0 = 0	Sum of 0 with a carry of 0
0 + 1 = 1	Sum of 1 with a carry of 0
1 + 0 = 1	Sum of 1 with a carry of 0
1 + 1 = 10	Sum of 0 with a carry of 1

Three basic digital circuits are used to perform in binary addition arithmetic functions are, the exclusive-OR gate (a.k.a. as a quarter-adder), the half-adder and the full-adder. Adders are important in computers and in other types of digital systems in which numerical data are processed. An understanding of the basic adder operation is fundamental to the study of digital systems. For this laboratory, the half-adder and full-adder are used.

HALF-ADDER

A half-adder accepts two binary digits on its inputs and produces two binary digits on its outputs namely a sum bit (∑) and carry bit (C_{out}). The half-adder is represented by the logic symbol as shown in Figure 1 and logic diagram as shown in Figure 2.

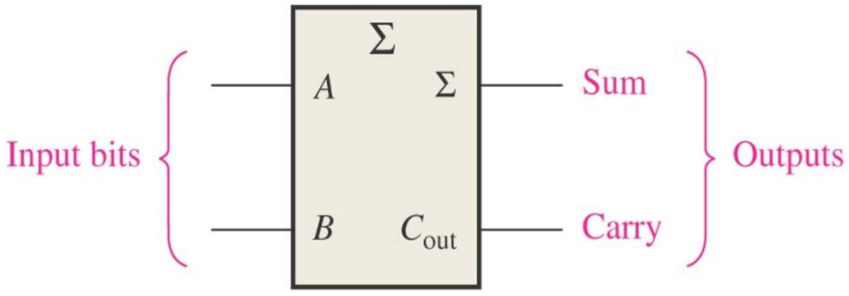

Figure 1: Logic symbol for a half-adder

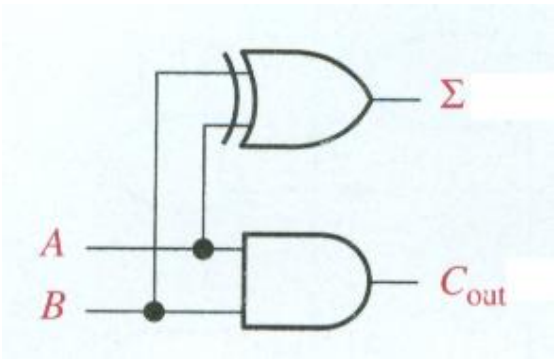

Figure 2: Half-adder logic diagram

FULL-ADDER

The full-adder accepts two input bits and an input carry and generates a sum output (∑) and the output carry (C_{out}). The basic difference between a full-adder and a half-adder is shown in Figure 3 and Figure 4 respectively.

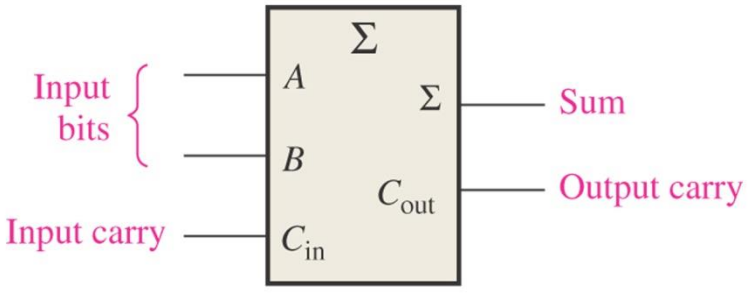

Figure 3: Logic symbol for a full-adder

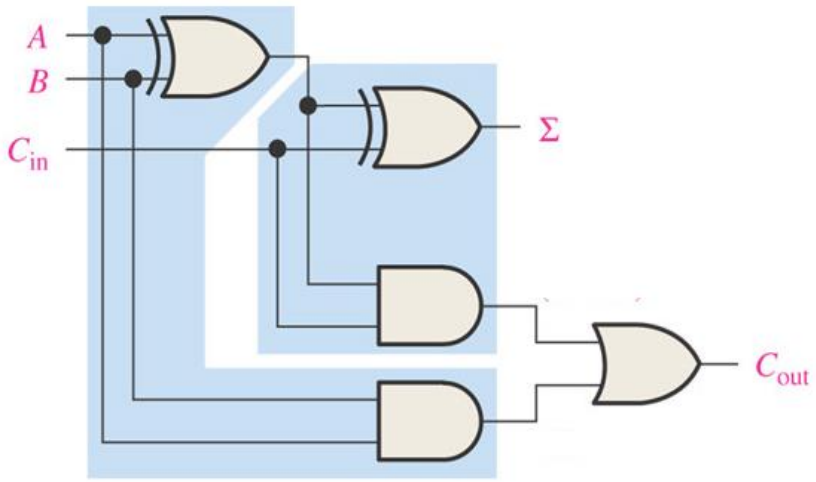

Figure 4: Full-adder logic diagram (each half-adder is enclosed by a shaded area)

PROCEDURE

PART A – HALF-ADDER

1. Construct a logic circuit as shown in Figure 2 and express the Boolean expression.
2. Develop a truth table based on the Boolean expression obtained in 1.
3. Demonstrate the solution and get approval from the lecturer or teaching engineer.

PART B – FULL-ADDER

1. Construct a logic circuit as shown in Figure 4 and express the Boolean expression.
2. Develop a truth table based on the Boolean expression obtained in 1.
3. Demonstrate the solution and get approval from the lecturer or teaching engineer.

PART C – DESIGN PROBLEM

Two or more full-adders are connected to form parallel binary adders. A single full-adder is capable of adding two 1-bit numbers and a input carry. To add binary with more than one bit, additional full-adders are used. Design a 2-bit parallel adder using the full-adder.

1. Draw a block diagram for a 2-bit parallel adder.
2. Draw a complete logic diagram for the 2-bit parallel adder.
3. Construct the logic circuit proposed in 2.
4. Demonstrate the solution and get approval from the lecturer or teaching engineer.

RESULT

PART A

1. Boolean expression of a half-adder and the equivalent truth table [3 marks]

   Boolean expression:

   Truth-table:

A	B	C_{out}	LED (ON/OFF)	$\sum$	LED (ON/OFF)

MARKS
DEMO: /10

PART B

1. Boolean expression of a full-adder and the equivalent truth table [3 marks]

   Boolean expression:

   Truth-table:

A	B	C_{in}	C_{out}	LED (ON/OFF)	$\sum$	LED (ON/OFF)

MARKS
DEMO: /10

PART C

MARKS	
DEMO:	/10

1. Block diagram of a 2-bit parallel adder. [3 marks]

2. Complete logic diagram for the 2-bit parallel adder. [3 marks]

3. Test your circuit by completing the table below [3 marks]

A_1	B_1	A_2	B_2	$\sum_3$	LED (ON/OFF)	$\sum_2$	LED (ON/OFF)	C_{out}	LED (ON/OFF)	$\sum_1$	LED (ON/OFF)
1	0	1	0								
1	1	1	1								
0	1	0	0								

DISCUSSION [3 marks]

CONCLUSION [2 marks]