MARKS	
DEMO:	
PART A:	/10
PART B:	/10
REPORT:	/35
TOTAL:	/55

UNIVERSITI MALAYSIA PERLIS

ENT 262
DIGITAL LOGIC DESIGN
SEMESTER 1 2019/2020

LABORATORY 4

MULTIPLEXER & DEMULTIPLEXER

Student's Particular

Name :
Matrix No :
Group :
Date of exp :
Breadboard No :

LAB 4: MULTIPLEXER & DEMULTIPLEXER

OBJECTIVES

1. To understand the operation of multiplexer and demultiplexer.
2. To design basic multiplexer and demultiplexer combinational circuit
3. To investigate the application of multiplexer and demultiplexer in a synchronous data transmission system.

EQUIPMENTS/COMPONENTS

- A DC power supply capable of 5V DC output
- Logic gates (74xx-series)
- Light Emitting Diodes (LED)
- 330 Ω resistor
- Switches

INTRODUCTION

A digital multiplexer (MUX) or data selector is a logic circuit that accepts several digital data inputs and selects one of them at any given time to pass on to the output. Primarily they are used for data routing which selects a transmission path for outgoing data according to the coding criteria established by binary inputs. The routing of the desired data input to the output is controlled by SELECT inputs (often referred to as ADDRESS inputs). Figure 1(a) shows the functional diagram of a general digital multiplexer.

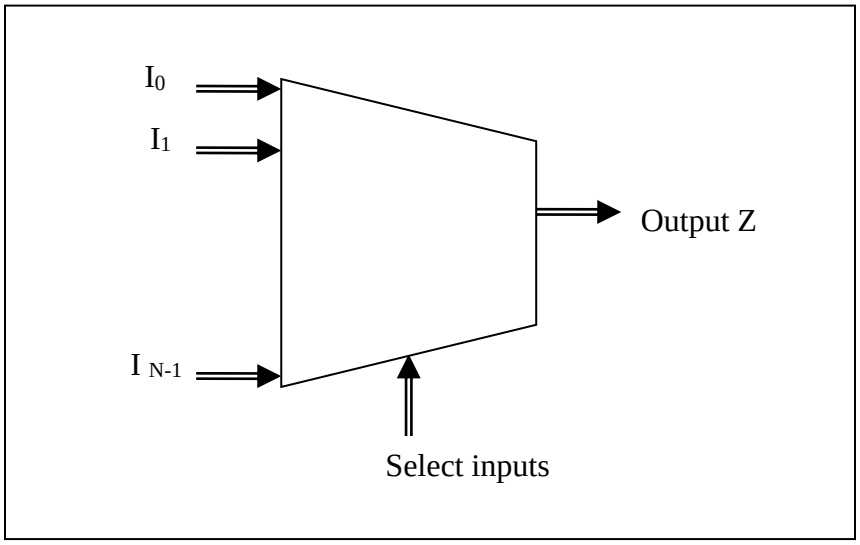


Figure 1(a) : Functional diagram of digital multiplexer (MUX)

A Multiplexer takes several inputs and transmits one of them to the output. A demultiplexer performs the reverse operations. It takes a single input and distributes it over several outputs. Figure 1(b) shows the functional diagram for digital demultiplexer (DEMUX). The select inputs code determines to which output the DATA input will be transmitted. In other words, the demultiplexer takes one input data sources and selectively distributes it to 1 of N output channels just like multiposition switch.

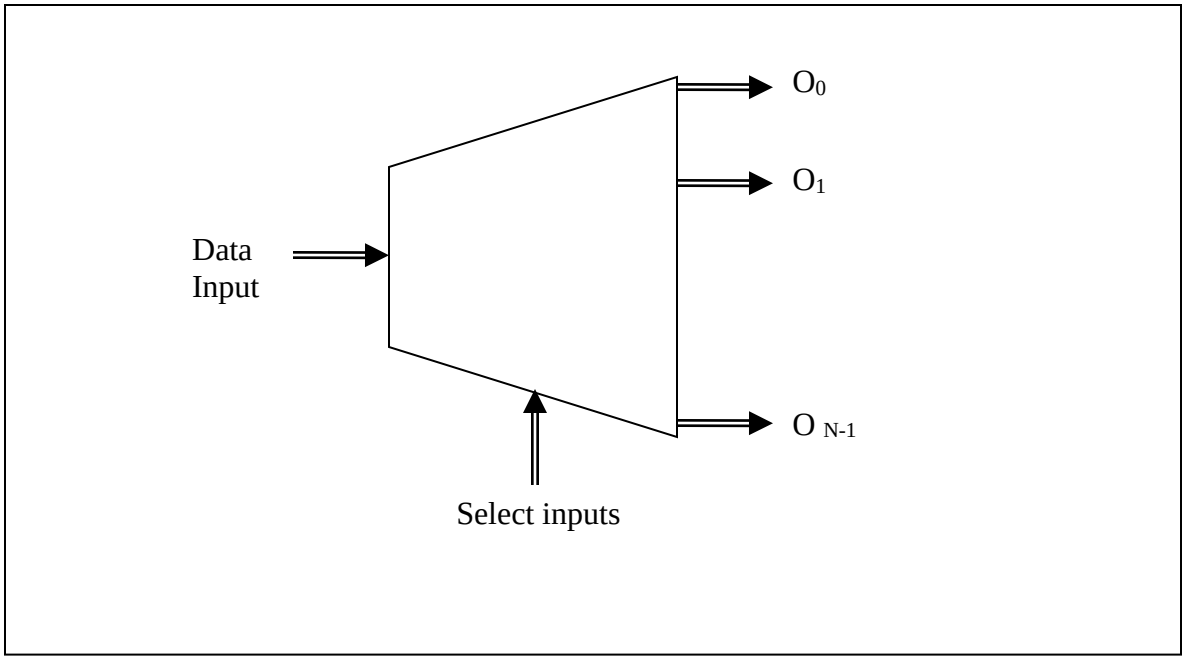


Figure 1(b) : General demultiplexer (DEMUX)

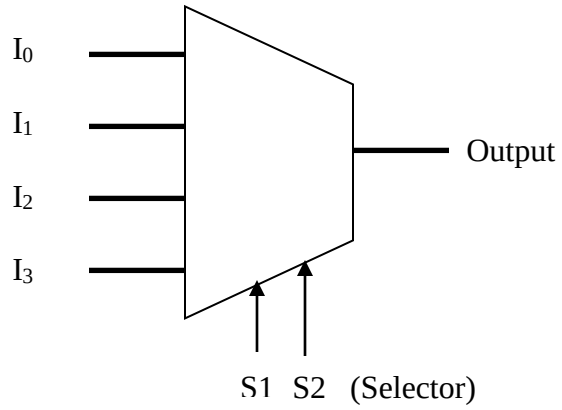
PROCEDURE

PART A

1. Figure 2 shows the logic diagram of 4:1 MUX and 1:4 DEMUX. Design both MUX and DEMUX by showing:

    a) Truth Table
    b) Boolean Expression
    c) Circuit Diagram

4 to 1 MUX



1 to 4 DEMUX

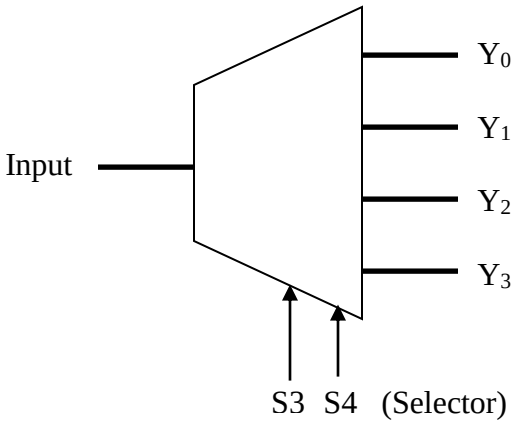


Figure 2: 4:1 MUX and 1:4 DEMUX

2. Construct the circuit for either MUX **OR** DEMUX that you have designed in procedure 1. Check the operation of the circuit and compare the result with the truth table .

PART B

1. Combine your circuit with your **partner** as shown in Figure 3 in order to investigate the application of MUX and DEMUX in a synchronous data transmission system.

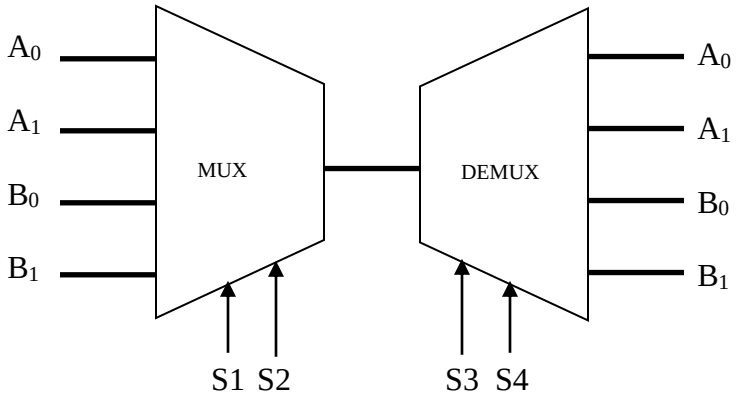


Figure 3: Combination MUX and DEMUX

RESULT

MARKS
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PART A

4:1 MUX

a) Truth Table [3 marks]

Selector		Input				Output
S_2	S_1	I_3	I_2	I_1	I_0	Q

b) Boolean Expression [2 marks]

c) Circuit Diagram [5 marks]

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1:4 DEMUX

a) Truth Table [3 marks]

Input Select		Output (Y)
S_4	S_3	

b) Boolean Expression [2 marks]

c) Circuit Diagram [5 marks]

PART B

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Record your observations of step 1 in below table.
[5 marks]

Inputs Select				**Output Observation** (Tick √ for ON LED)			
S_4	**S_3**	**S_2**	**S_1**	**LED 1**	**LED 2**	**LED 3**	**LED 4**

DESIGN PROBLEM

Proof that 4:1 MUX can be use to form an 8:1 MUX. Your design should use 4:1 MUX and logic gates (74XXX series) ONLY. (use block diagram(4:1 MUX) as shown in Figure 2) [5 marks]

DISCUSSION [3 marks]

CONCLUSION [2 marks]