MARKS
DEMO: /10
REPORT: /30
TOTAL: /40

ENT 262
DIGITAL LOGIC DESIGN
SEMESTER 1 2019/2020

LABORATORY 6

COUNTER DESIGN

Student's Particular

Name :
Matrix No :
Group :
Date of exp :
Breadboard No :

LAB 6: COUNTER DESIGN

OBJECTIVES:

1. To investigate and analyze the operation of JK flip-flop.
2. To design different flip-flop using JK flip-flop.
3. To design a synchronous counter using JK flip-flops.

EQUIPMENTS/COMPONENTS

- Logic gates (74XX-series)
- J-K flip- flop (7476)
- LED monitor
- Oscilloscope
- Signal Generator

INTRODUCTION

A counter is a digital sequential logic device that will go through a certain predefined state based on the application of the input pulses. There are two main types of counters: Asynchronous Counter and Synchronous Counter. The counter utilizes flip-flop to store binary information, where the number of flip-flops used will determine the capability of counting bits.

In this experiment, the students will design a Synchronous Counter using JK flip-flops which shown in Figure 6.1.

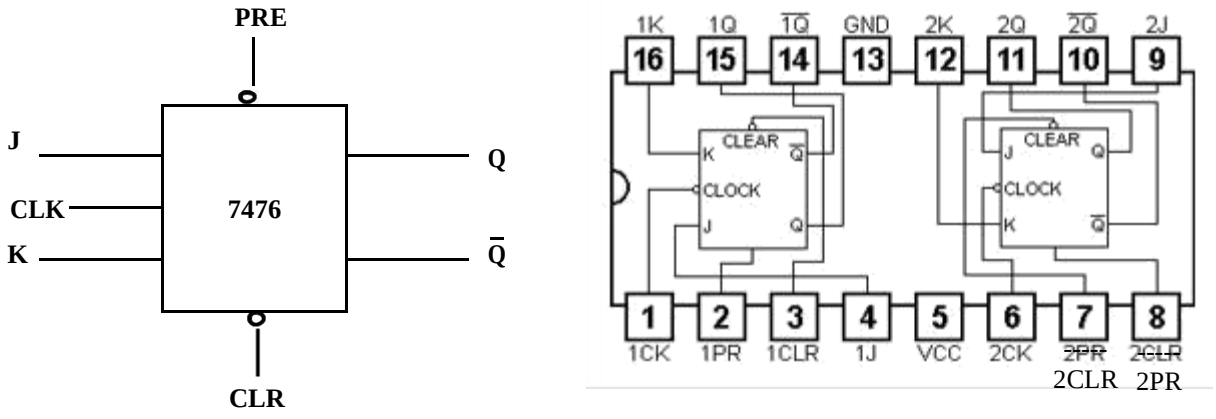

Figure 6.1 IC 7476 Series

TASKS

1. Investigate and analyze the operation of JK flip-flop by providing the truth table.

2. Design a Synchronous Counter based on the given sequence provided by instructor using JK flip-flops. Show all steps taken to design the counter and provide a sample of output waveform from the experiment for a cycle.

METHODOLOGY AND RESULTS [25 marks]

MARKS
DEMO: /10

DISCUSSION [3 marks]

1. Based on your investigation on JK flip-flop, discuss the function of CLR and PRE to a JK flip-flop. In addition, discuss what is observed when CLR and PRE input are activated in a counter.

2. Discuss the actual results obtained from the experiment and the sequence given by the instructor.

CONCLUSION [2 marks]